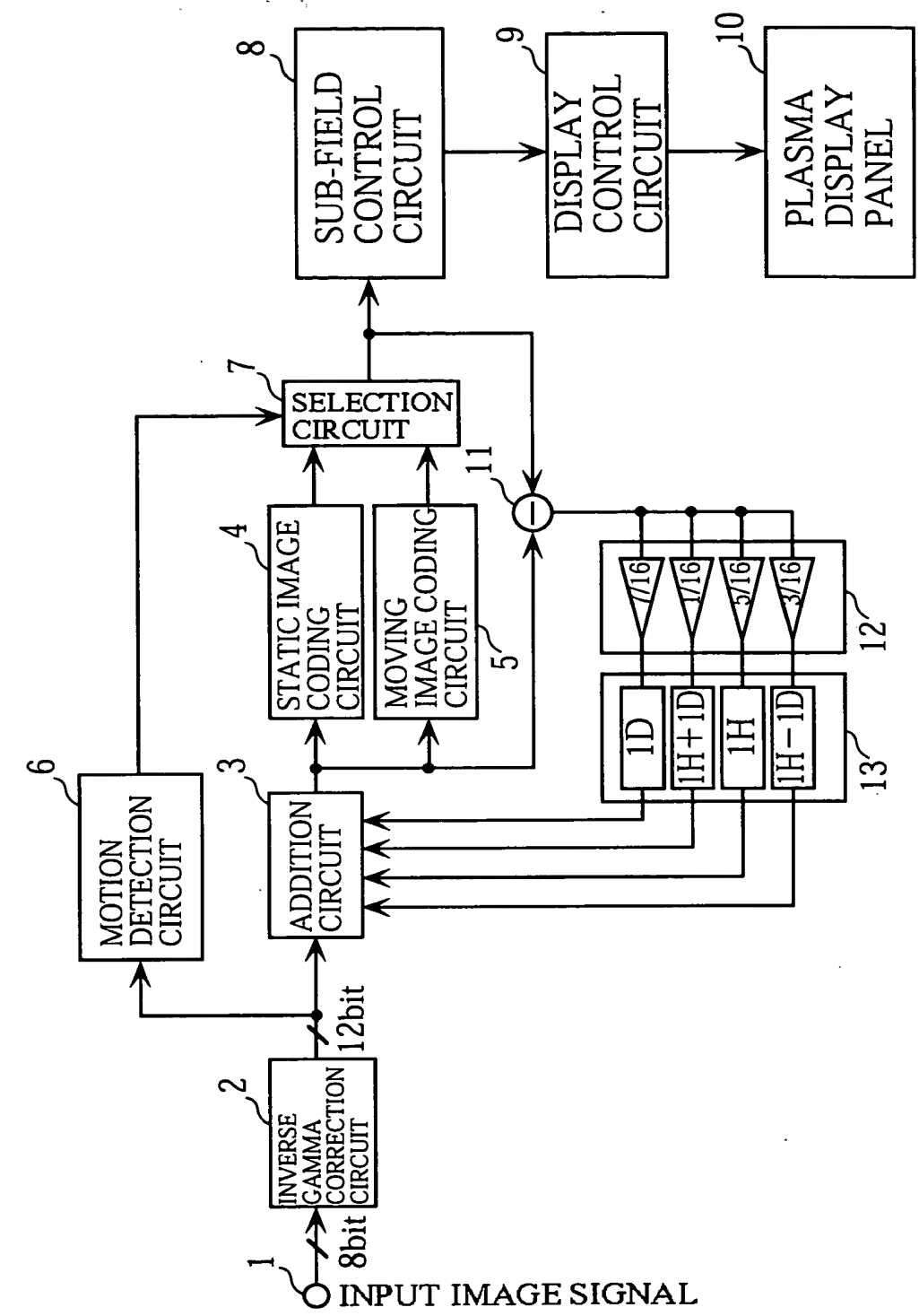

INPUT IMAGE SIGNAL
8bit
12bit
INVERSE GAMMA CORRECTION CIRCUIT
ADDITION CIRCUIT
MOTION DETECTION CIRCUIT
STATIC IMAGE CODING CIRCUIT
MOVING IMAGE CODING CIRCUIT
SELECTION CIRCUIT
SUB-FIELD CONTROL CIRCUIT
DISPLAY CONTROL CIRCUIT
PLASMA DISPLAY PANEL
1D
1H+1D
1H
1H−1D
1/16
1/16
3/16
3/16
1
2
3
4
5
6
7
8
9
10
11
12
13

FIG.1

FIG.2

INPUT IMAGE SIGNAL	STATIC IMAGE CODING
0	0
1	1
2	2
3	3
4	5
5	5
6	6
:	:
9	10
10	10
11	11
12	12
13	13
14	15
15	15
16	16
:	:
20	20
30	30
40	40
50	50
60	60
70	70
80	80
91	91
101	101
111	111
119	119
130	130
140	140
150	150
160	160
170	170
180	180
191	191
201	201
211	211
221	221
231	231
240	240
250	250
260	260
273	273
283	283
293	293
300	300
310	310
320	320
330	330
340	340
350	350
360	360
370	370
380	380

41

41

41

FIG.3

INPUT IMAGE SIGNAL	MOVING IMAGE CODING
0	0
1	1
2	2
3	3
4	5
5	5
6	6
:	:
9	10
10	10
11	11
12	12
13	13
14	15
15	15
16	16
:	:
20	20
30	30
40	
50	
60	60
70	
80	
91	91
101	101
111	111
119	119
130	
140	
150	150
160	160
170	170
180	180
191	
201	
211	
221	221
231	231
240	240
250	250
260	260
273	
283	
293	
300	300
310	310
320	320
330	330
340	340
350	350
360	360
370	370
380	380

51

51

51

52

52

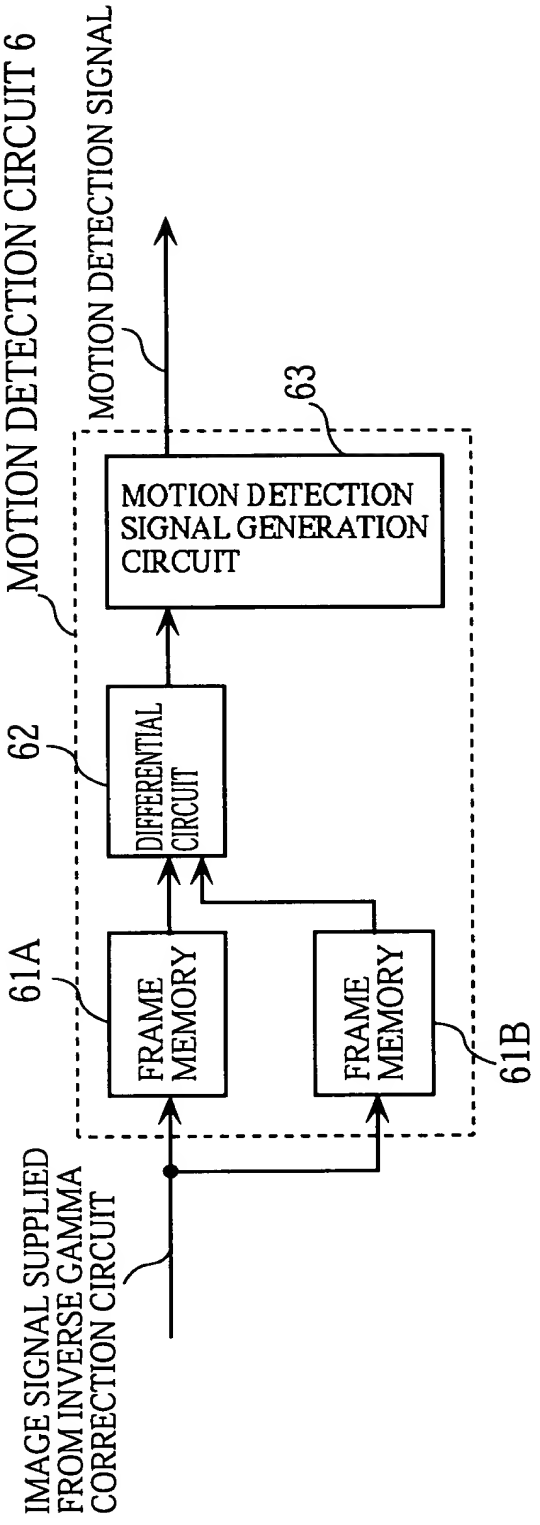

MOTION DETECTION CIRCUIT 6
MOTION DETECTION SIGNAL
63
MOTION DETECTION SIGNAL GENERATION CIRCUIT
62
DIFFERENTIAL CIRCUIT
61A
FRAME MEMORY
FRAME MEMORY
61B
IMAGE SIGNAL SUPPLIED FROM INVERSE GAMMA CORRECTION CIRCUIT

FIG.4

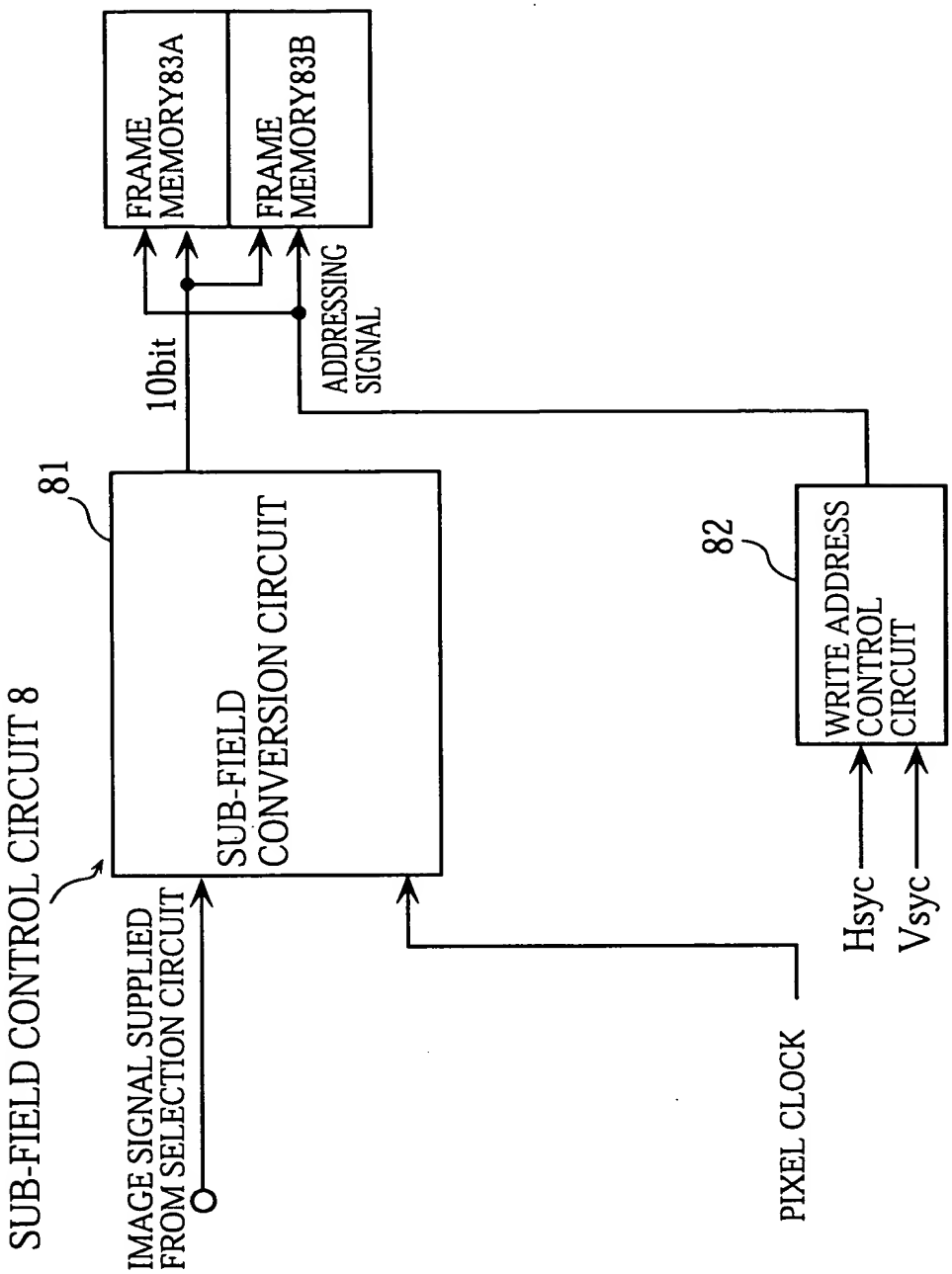

SUB-FIELD CONTROL CIRCUIT 8
81
SUB-FIELD
CONVERSION CIRCUIT
IMAGE SIGNAL SUPPLIED
FROM SELECTION CIRCUIT
10bit
FRAME
MEMORY83A
FRAME
MEMORY83B
ADDRESSING
SIGNAL
82
WRITE ADDRESS
CONTROL
CIRCUIT
Hsyc
Vsyc
PIXEL CLOCK

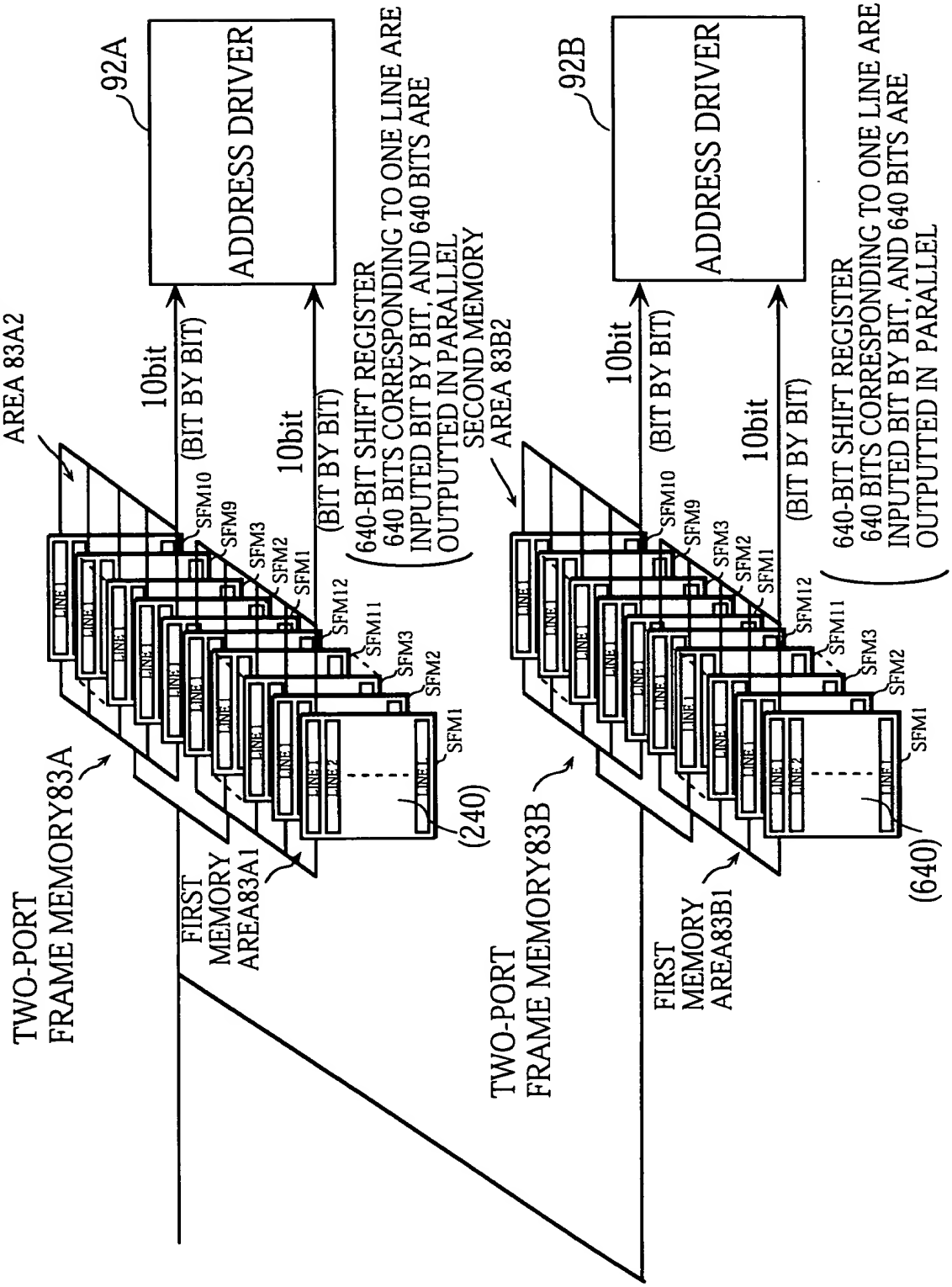
FIG.5

FIG.6

INPUT IMAGE SIGNAL	LUMINANCE WEIGHT									
	1(SF1)	2(SF2)	5(SF3)	10(SF4)	20(SF5)	33(SF6)	48(SF7)	66(SF8)	87(SF9)	111(SF10)
0										
1	1									
2		1								
3	1	1								
5			1							
6	1		1							
:										
10				1						
11	1			1						
12		1		1						
13	1	1		1						
15			1	1						
16			1	1						
:										
20					1					
30				1	1					
40		1	1			1				
50		1	1	1		1				
60		1	1		1	1				
70		1			1		1			
80		1		1	1		1			
91				1		1	1			
101					1	1	1			
111				1	1	1	1			
119	1	1	1	1	1	1	1			
130	1			1	1	1		1		
140	1		1		1		1	1		
150	1	1				1	1	1		
160	1	1		1		1	1	1		
170	1	1			1	1	1	1		
180	1	1		1	1	1	1	1		
191	1	1			1	1	1		1	
201	1	1		1	1	1	1		1	
211			1		1	1		1	1	
221					1		1	1	1	
231				1	1		1	1	1	
240	1		1			1	1	1	1	
250	1		1	1		1	1	1	1	
260	1		1		1	1	1	1	1	
273			1	1		1	1	1		1
283			1		1	1	1	1		1
293			1	1	1	1	1	1		1
300	1	1				1		1	1	1
310	1	1		1		1		1	1	1
320	1	1			1	1		1	1	1
330	1	1		1	1	1		1	1	1
340	1	1	1		1		1	1	1	1
350			1			1	1	1	1	1
360			1	1		1	1	1	1	1
370			1		1	1	1	1	1	1
380			1	1	1	1	1	1	1	1

84

FIG.7


92A
ADDRESS DRIVER
92B
ADDRESS DRIVER
10bit
(BIT BY BIT)
10bit
(BIT BY BIT)
640-BIT SHIFT REGISTER
640 BITS CORRESPONDING TO ONE LINE ARE
INPUTED BIT BY BIT, AND 640 BITS ARE
OUTPUTTED IN PARALLEL
SECOND MEMORY
AREA 83A2
SECOND MEMORY
AREA 83B2
TWO-PORT
FRAME MEMORY83A
TWO-PORT
FRAME MEMORY83B
FIRST
MEMORY
AREA83A1
FIRST
MEMORY
AREA83B1
SFM1
SFM2
SFM3
SFM9
SFM10
SFM11
SFM12
(240)
(640)

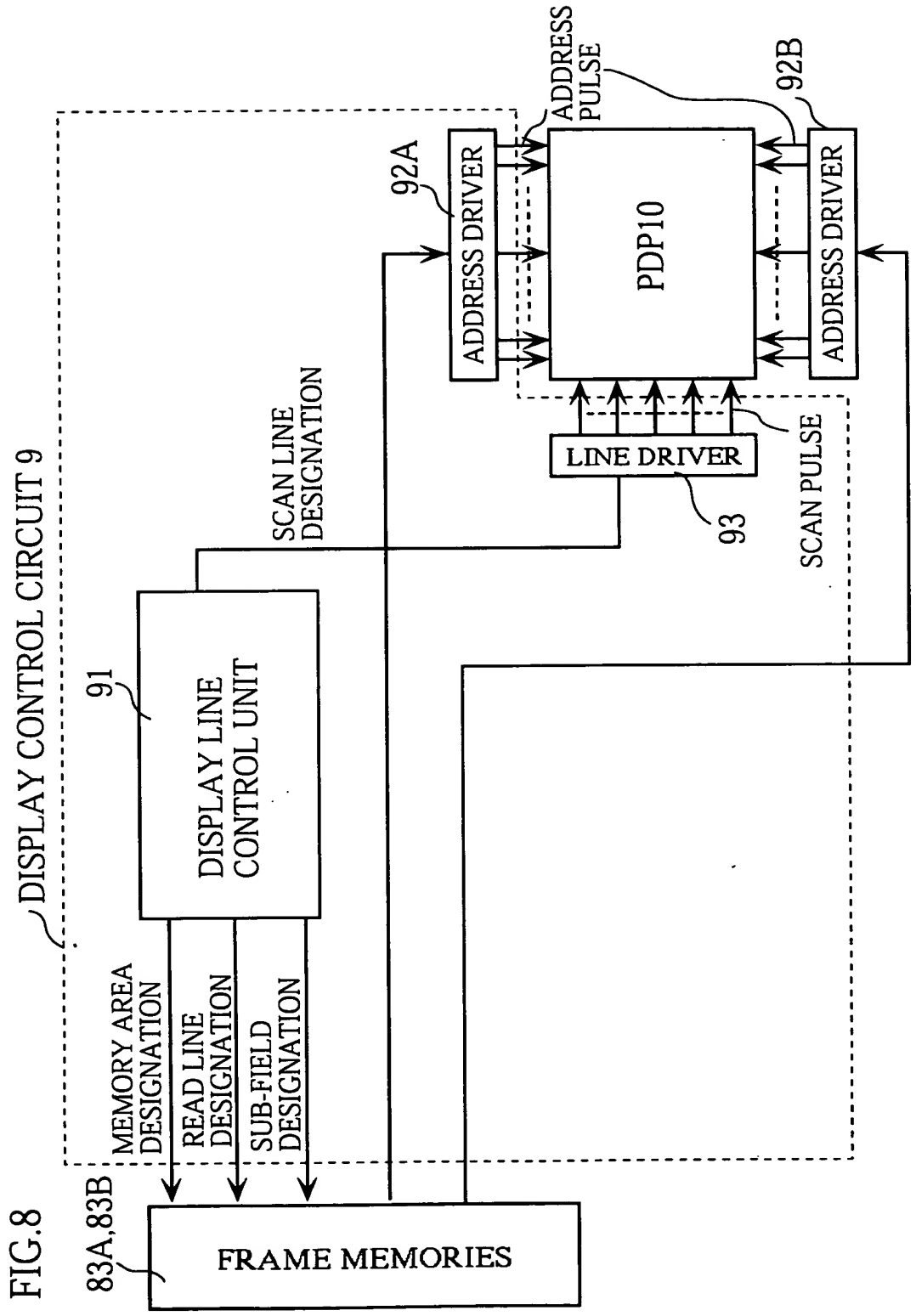

DISPLAY CONTROL CIRCUIT 9
91
DISPLAY LINE CONTROL UNIT
SCAN LINE DESIGNATION
92A
ADDRESS DRIVER
ADDRESS PULSE
92B
ADDRESS DRIVER
PDP10
LINE DRIVER
93
SCAN PULSE
MEMORY AREA DESIGNATION
READ LINE DESIGNATION
SUB-FIELD DESIGNATION
83A,83B
FRAME MEMORIES

FIG.8

FIG. 9

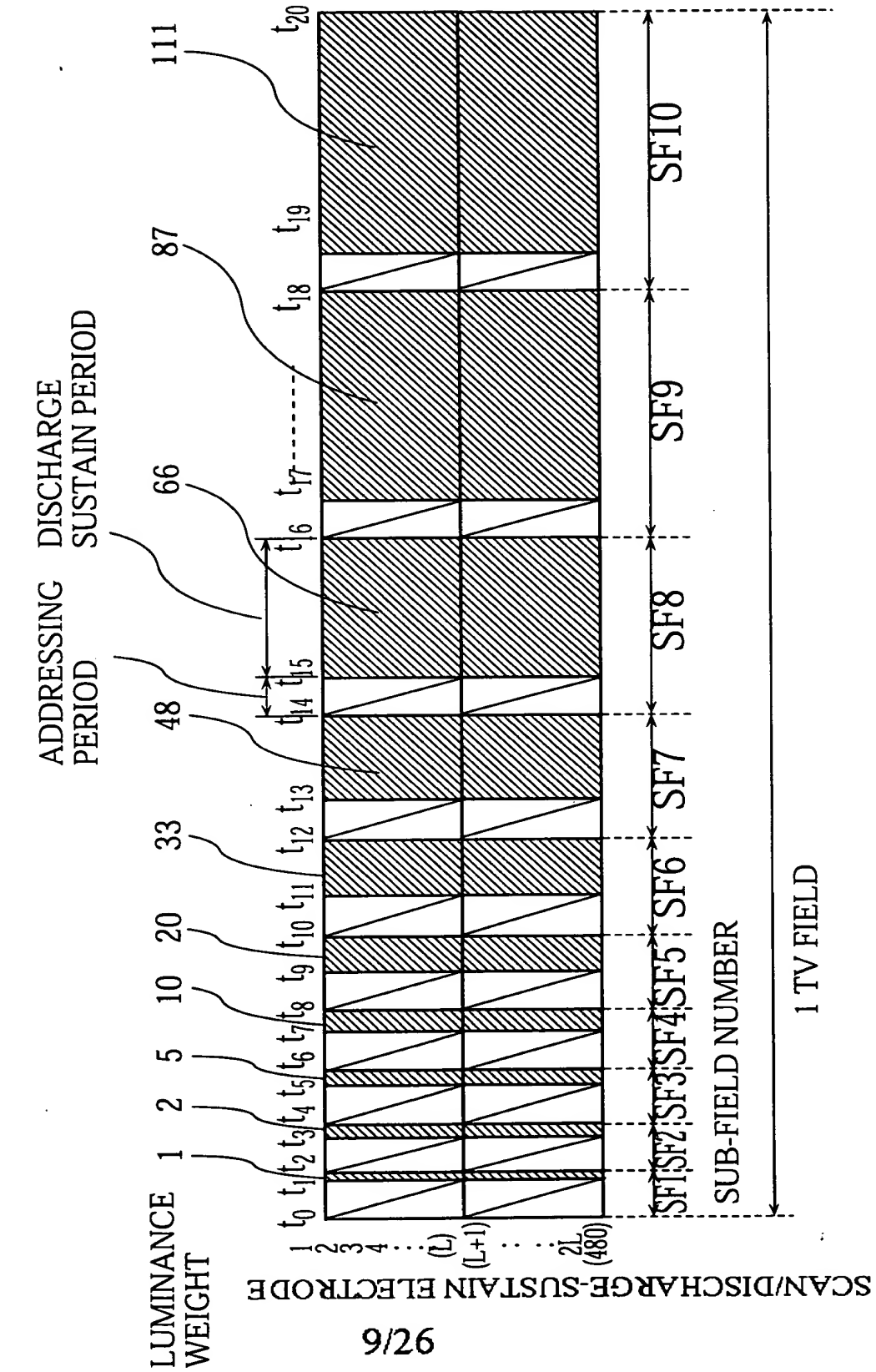
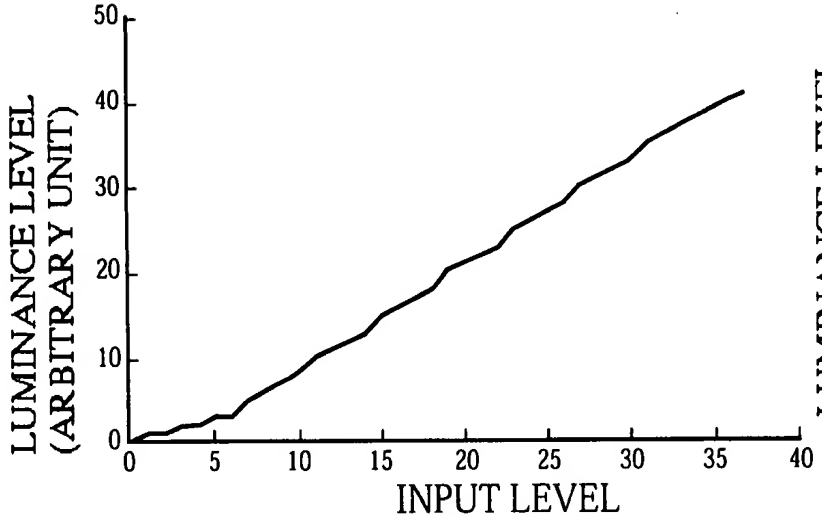

LUMINANCE WEIGHT
1
2
5
10
20
33
48
66
87
111
ADDRESSING PERIOD
DISCHARGE SUSTAIN PERIOD
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
SF9
SF10
SUB-FIELD NUMBER
1 TV FIELD
SCAN/DISCHARGE-SUSTAIN ELECTRODE
1
2
3
4
(L)
(L+1)
2L
(480)

FIG.10

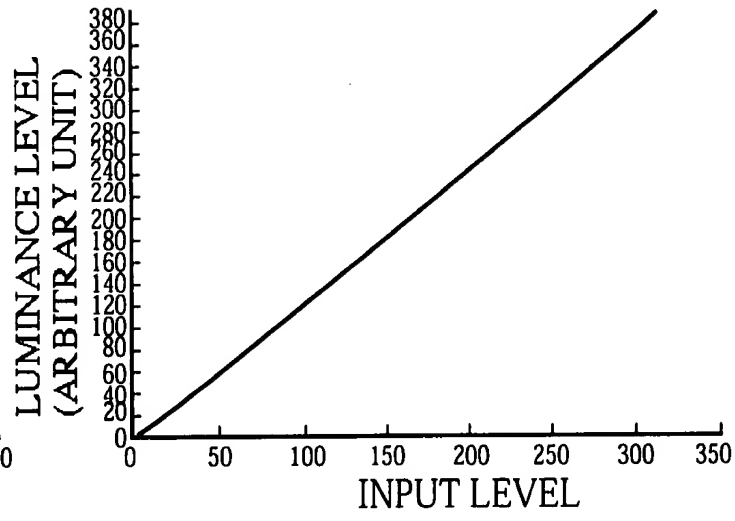
(a)

INPUT LEVEL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
LUMINANCE LEVEL	0	1	1	2	2	3	3	5	6	7	8	10	11	12	13	15	16	17	18	20	21	22	23	25	26	27	28	30	31	32	33	35	36	37	38	39	40	41

(b)



(c)



09/701753

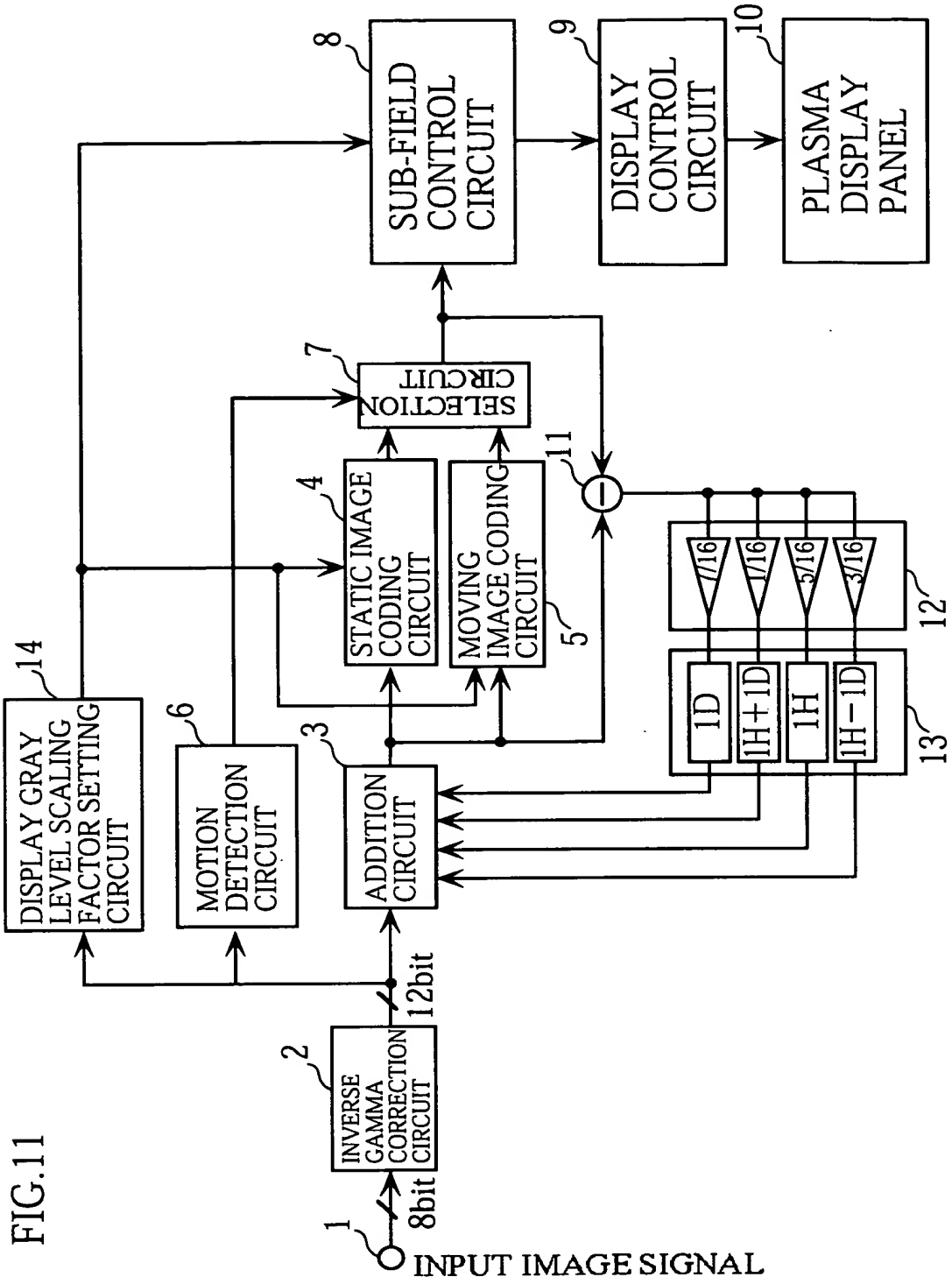

INPUT IMAGE SIGNAL
8bit
12bit
INVERSE GAMMA CORRECTION CIRCUIT
ADDITION CIRCUIT
MOTION DETECTION CIRCUIT
DISPLAY GRAY LEVEL SCALING FACTOR SETTING CIRCUIT
STATIC IMAGE CODING CIRCUIT
MOVING IMAGE CODING CIRCUIT
SELECTION CIRCUIT
SUB-FIELD CONTROL CIRCUIT
DISPLAY CONTROL CIRCUIT
PLASMA DISPLAY PANEL
1D
1H+1D
1H
1H−1D
7/16
7/16
5/16
3/16
1
2
3
4
5
6
7
8
9
10
11
12
13
14

FIG.11

FIG.12

(a) K=1

INPUT IMAGE SIGNAL	SF1 1	SF2 2	SF3 3	SF4 6	SF5 10
0					
1	1				
2		1			
3	1	1			
4	1		1		
5		1	1		
6	1	1	1		
7	1			1	
8		1		1	
9	1	1		1	
10	1		1	1	
11		1	1	1	
12	1	1	1	1	
13	1	1			1
14	1		1		1
15		1	1		1
16	1	1	1		1
17	1			1	1
18		1		1	1
19	1	1		1	1
20	1		1	1	1
21		1	1	1	1
22	1	1	1	1	1

(b) K=2

INPUT IMAGE SIGNAL	SF1 2	SF2 4	SF3 6	SF4 12	SF5 20
0					
2	1				
4		1			
6	1	1			
8	1		1		
10		1	1		
12	1	1	1		
14	1			1	
16		1		1	
18	1	1		1	
20	1		1	1	
22		1	1	1	
24	1	1	1	1	
26	1	1			1
28	1		1		1
30		1	1		1
32	1	1	1		1
34	1			1	1
36		1		1	1
38	1	1		1	1
40	1		1	1	1
42		1	1	1	1
44	1	1	1	1	1

(c) K=3

INPUT IMAGE SIGNAL	SF1 3	SF2 6	SF3 9	SF4 18	SF5 30
0					
3	1				
6		1			
9	1	1			
12	1		1		
15		1	1		
18	1	1	1		
21	1			1	
24		1		1	
27	1	1		1	
30	1		1	1	
33		1	1	1	
36	1	1	1	1	
39	1	1			1
42	1		1		1
45		1	1		1
48	1	1	1		1
51	1			1	1
54		1		1	1
57	1	1		1	1
60	1		1	1	1
63		1	1	1	1
66	1	1	1	1	1

(d) K=4

INPUT IMAGE SIGNAL	SF1 4	SF2 12	SF3 12	SF4 24	SF5 40
0					
4	1				
8		1			
12	1	1			
16	1		1		
20		1	1		
24	1	1	1		
28	1			1	
32		1		1	
36	1	1		1	
40	1		1	1	
44		1	1	1	
48	1	1	1	1	
52	1	1			1
56	1		1		1
60		1	1		1
64	1	1	1		1
68	1			1	1
72		1		1	1
76	1	1		1	1
80	1		1	1	1
84		1	1	1	1
88	1	1	1	1	1

(e) K=5

INPUT IMAGE SIGNAL	SF1 5	SF2 10	SF3 15	SF4 30	SF5 50
0					
5	1				
10		1			
15	1	1			
20	1		1		
25		1	1		
30	1	1	1		
35	1			1	
40		1		1	
45	1	1		1	
50	1		1	1	
55		1	1	1	
60	1	1	1	1	
65	1	1			1
70	1		1		1
75		1	1		1
80	1	1	1		1
85	1			1	1
90		1		1	1
95	1	1		1	1
100	1		1	1	1
105		1	1	1	1
110	1	1	1	1	1

09/701753

FIG.13

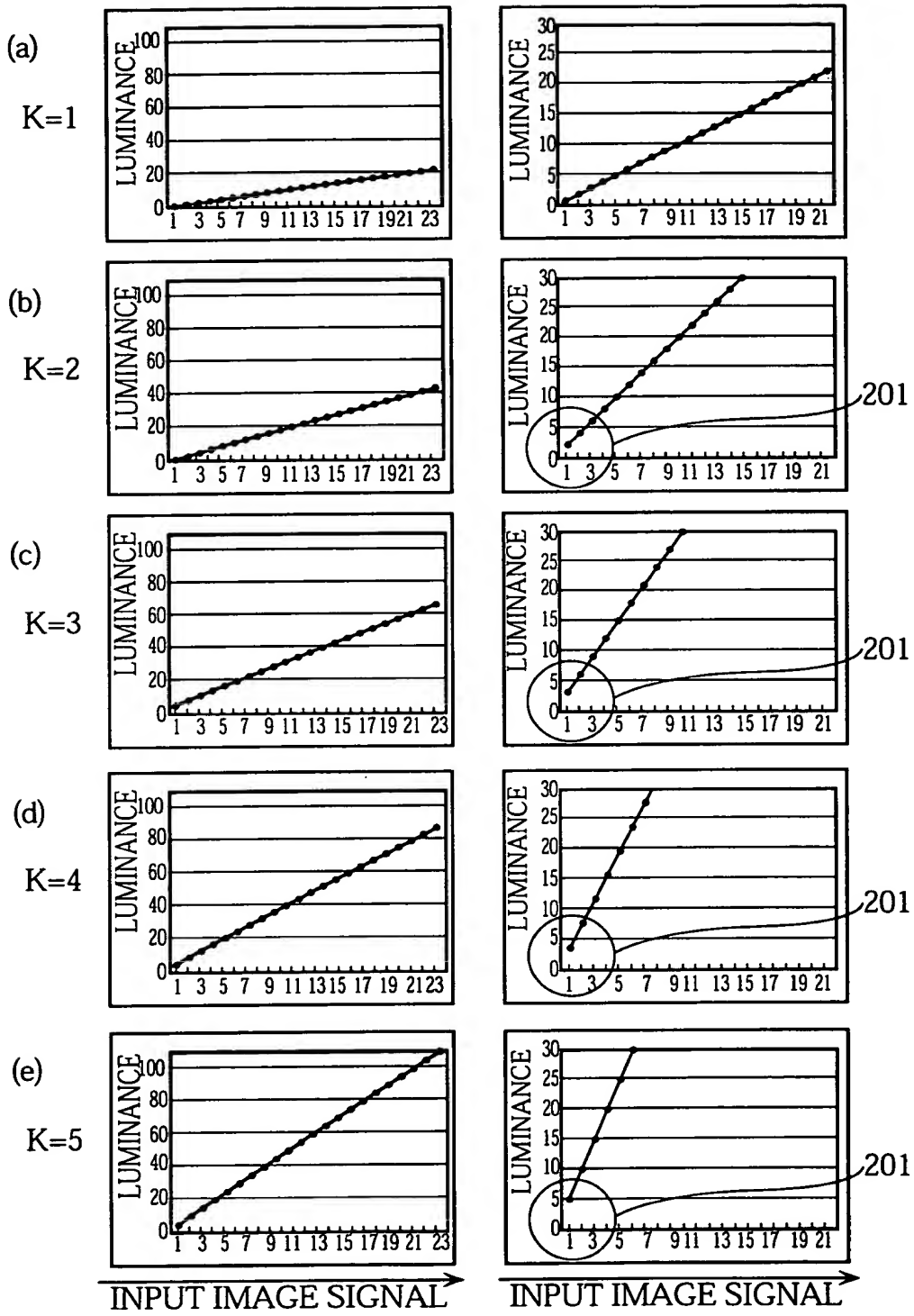


FIG.14

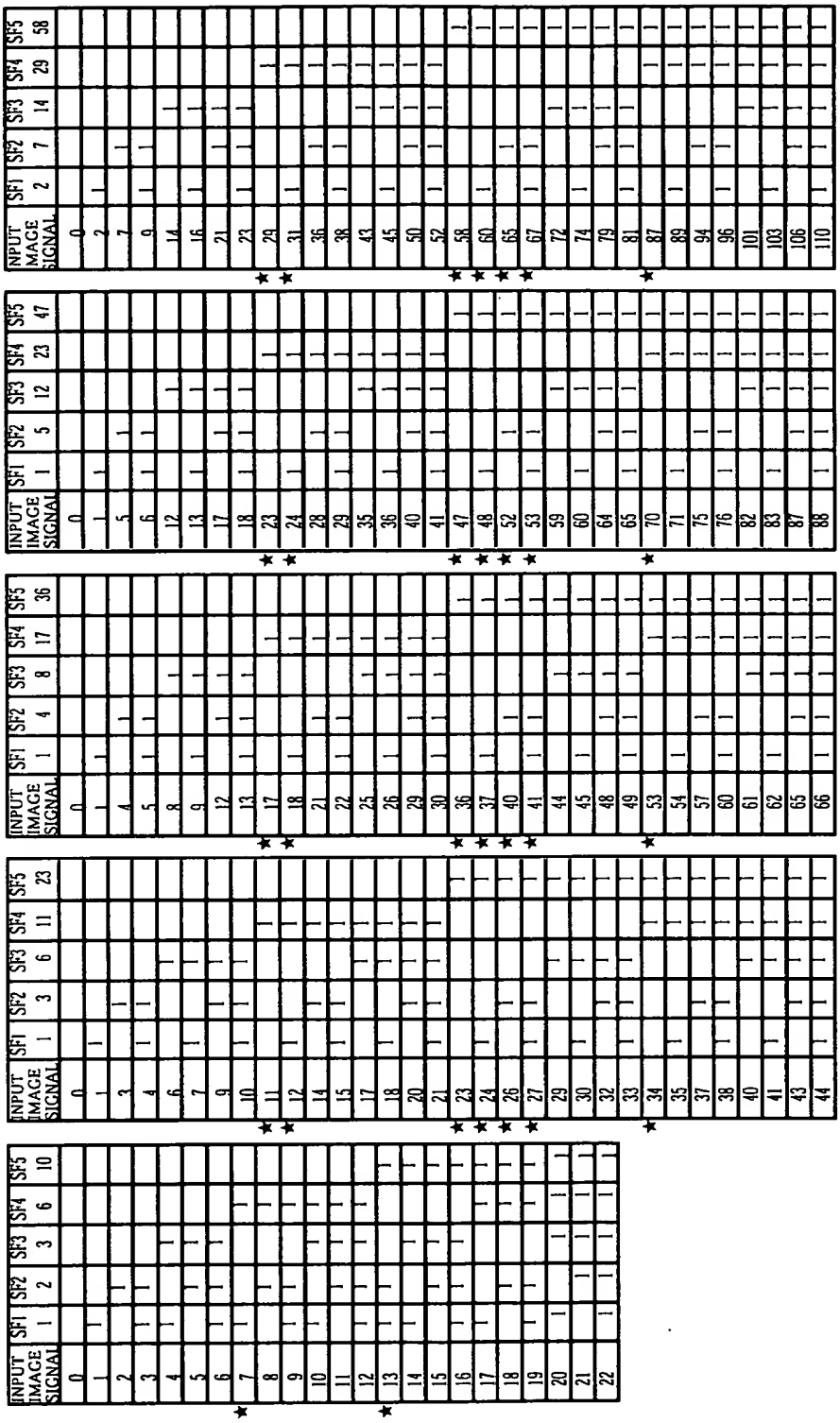
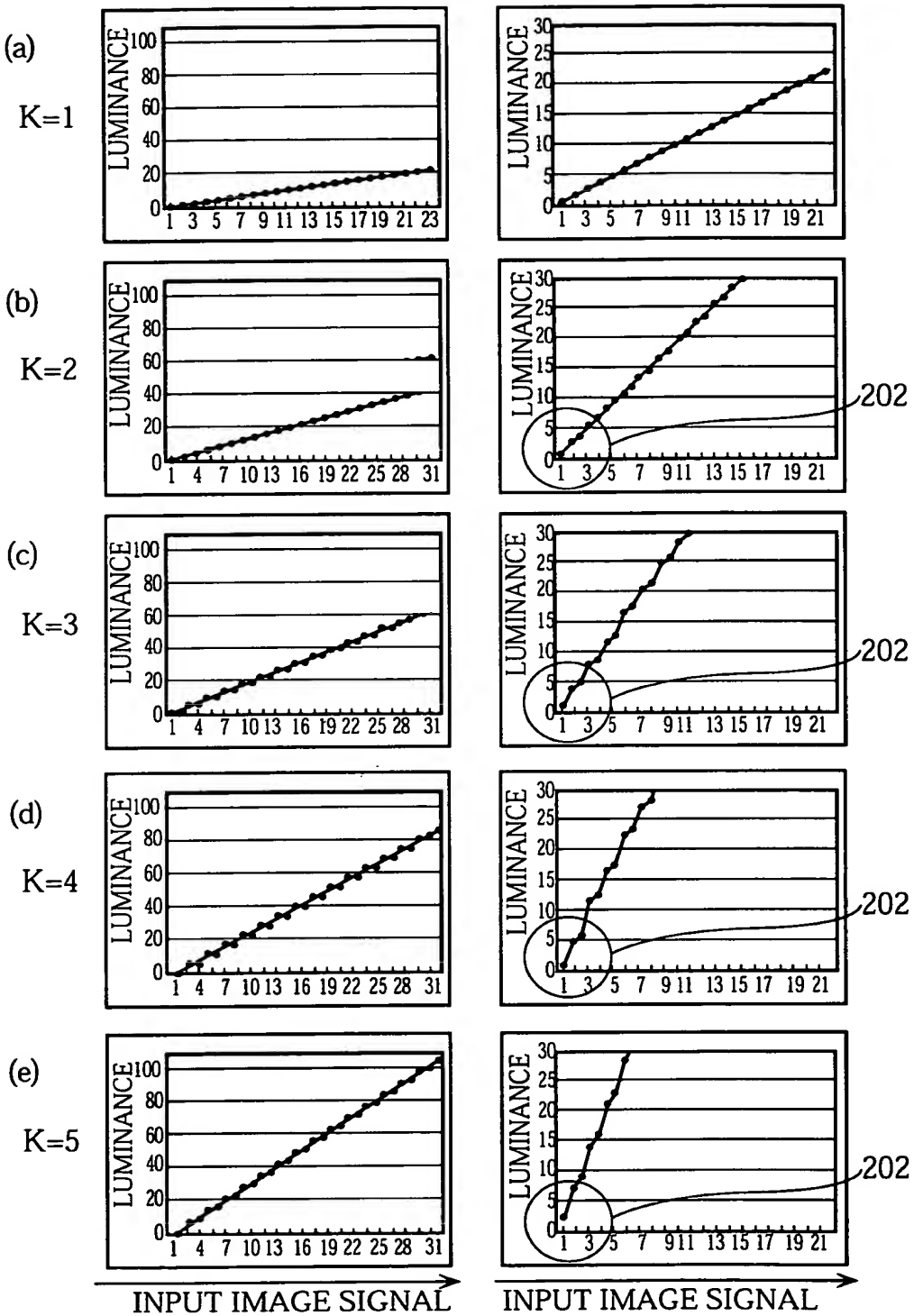


FIG.15



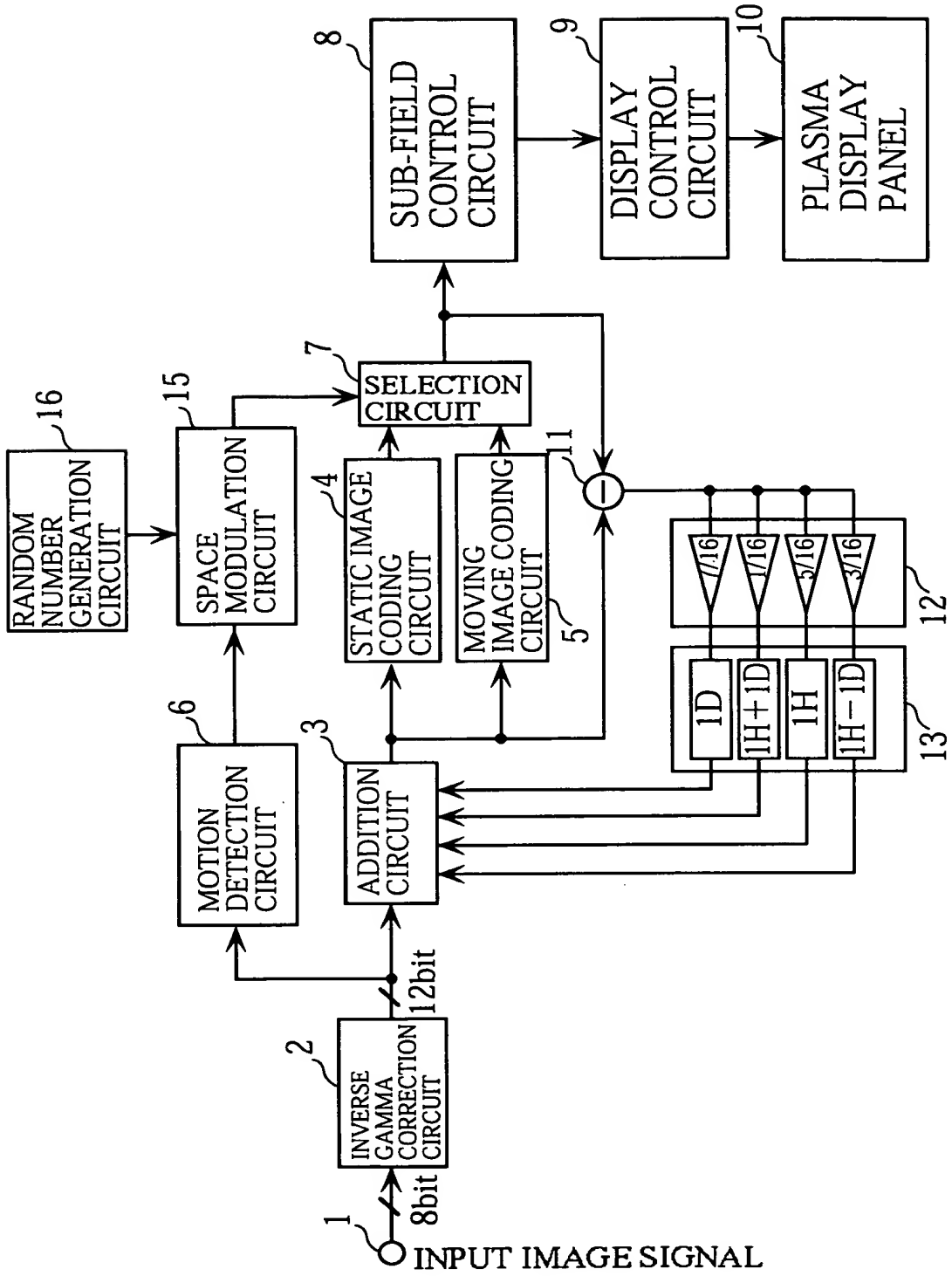

INPUT IMAGE SIGNAL
8bit
12bit
INVERSE GAMMA CORRECTION CIRCUIT
MOTION DETECTION CIRCUIT
ADDITION CIRCUIT
STATIC IMAGE CODING CIRCUIT
MOVING IMAGE CODING CIRCUIT
SELECTION CIRCUIT
SPACE MODULATION CIRCUIT
RANDOM NUMBER GENERATION CIRCUIT
SUB-FIELD CONTROL CIRCUIT
DISPLAY CONTROL CIRCUIT
PLASMA DISPLAY PANEL
7/16
7/16
5/16
3/16
1D
1H+1D
1H
1H−1D
1
2
3
4
5
6
7
8
9
10
11
12
13
15
16

FIG. 16

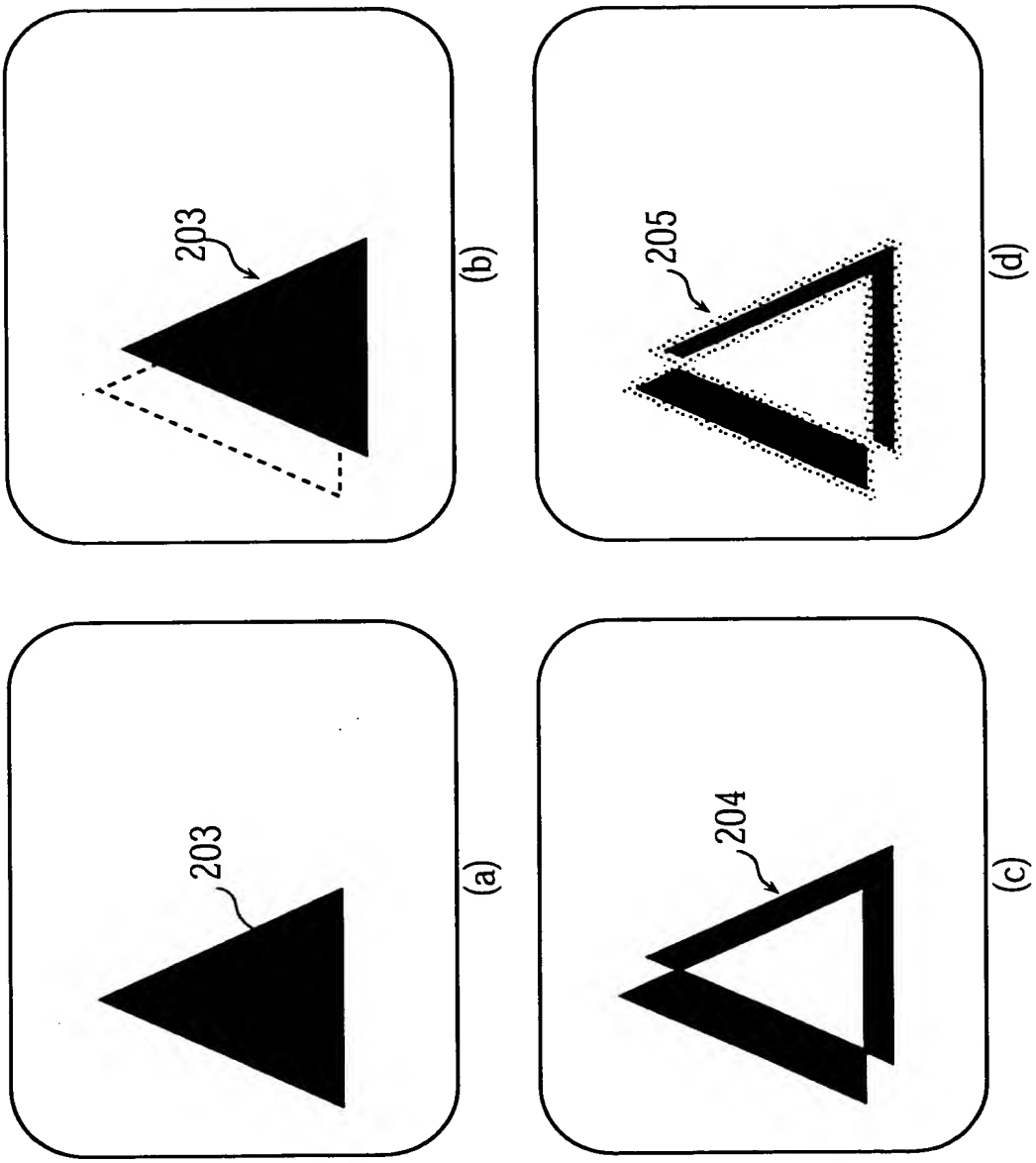


FIG.17

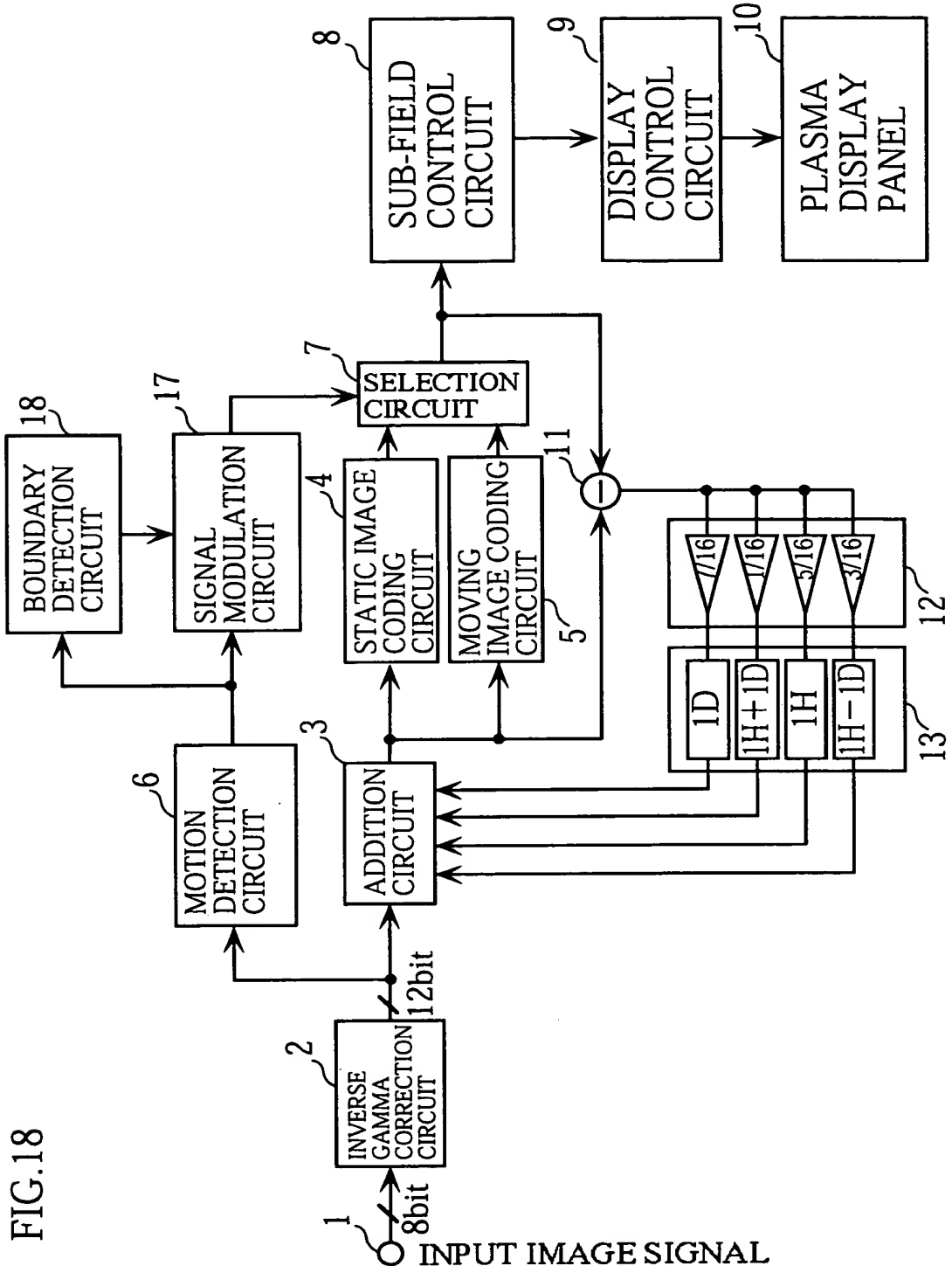

1
8bit
INPUT IMAGE SIGNAL
2
INVERSE GAMMA CORRECTION CIRCUIT
12bit
3
ADDITION CIRCUIT
6
MOTION DETECTION CIRCUIT
4
STATIC IMAGE CODING CIRCUIT
5
MOVING IMAGE CODING CIRCUIT
7
SELECTION CIRCUIT
17
SIGNAL MODULATION CIRCUIT
18
BOUNDARY DETECTION CIRCUIT
11
12
7/16
7/16
5/16
3/16
13
1D
1H+1D
1H
1H−1D
8
SUB-FIELD CONTROL CIRCUIT
9
DISPLAY CONTROL CIRCUIT
10
PLASMA DISPLAY PANEL

FIG.18

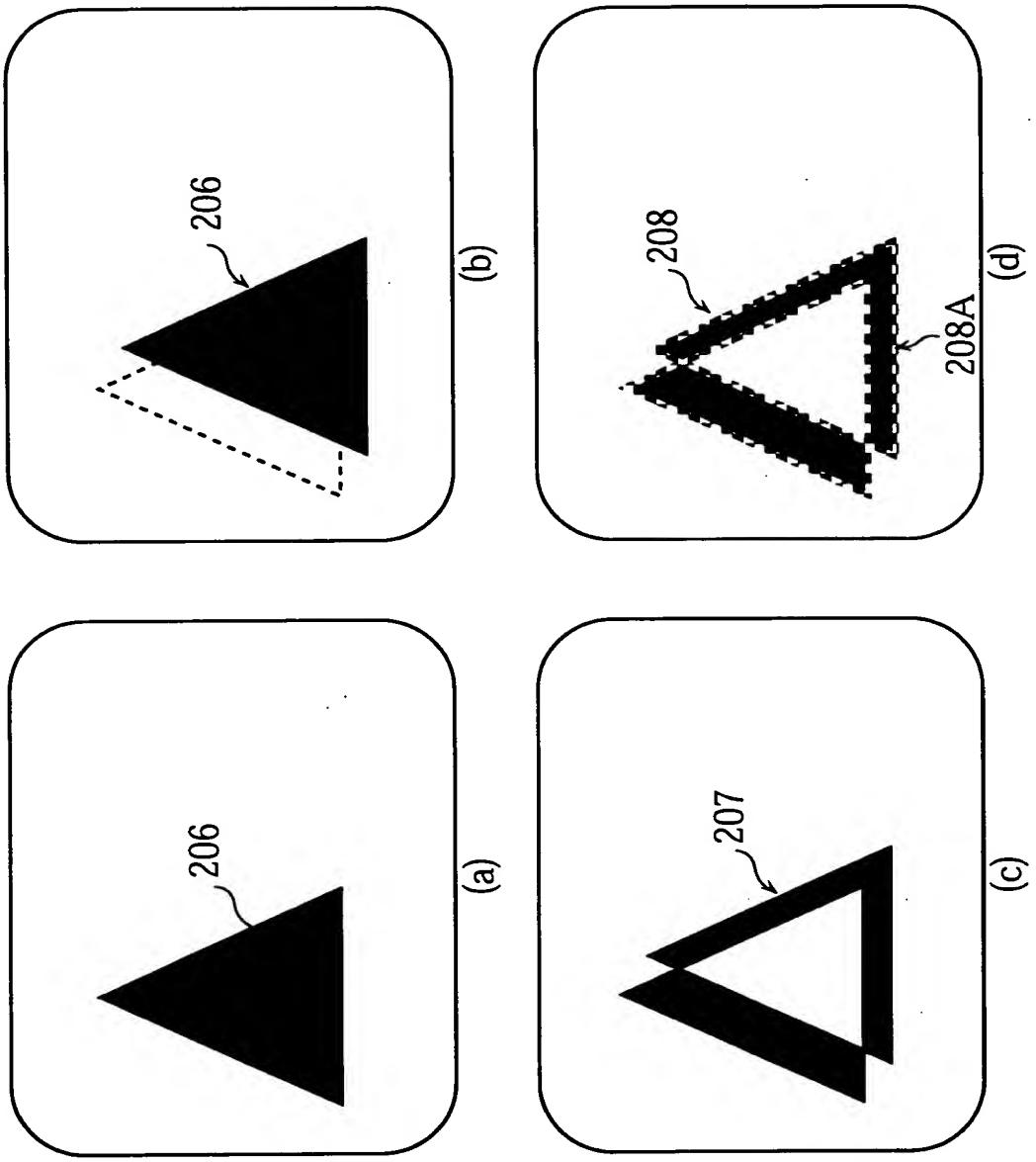


FIG.19

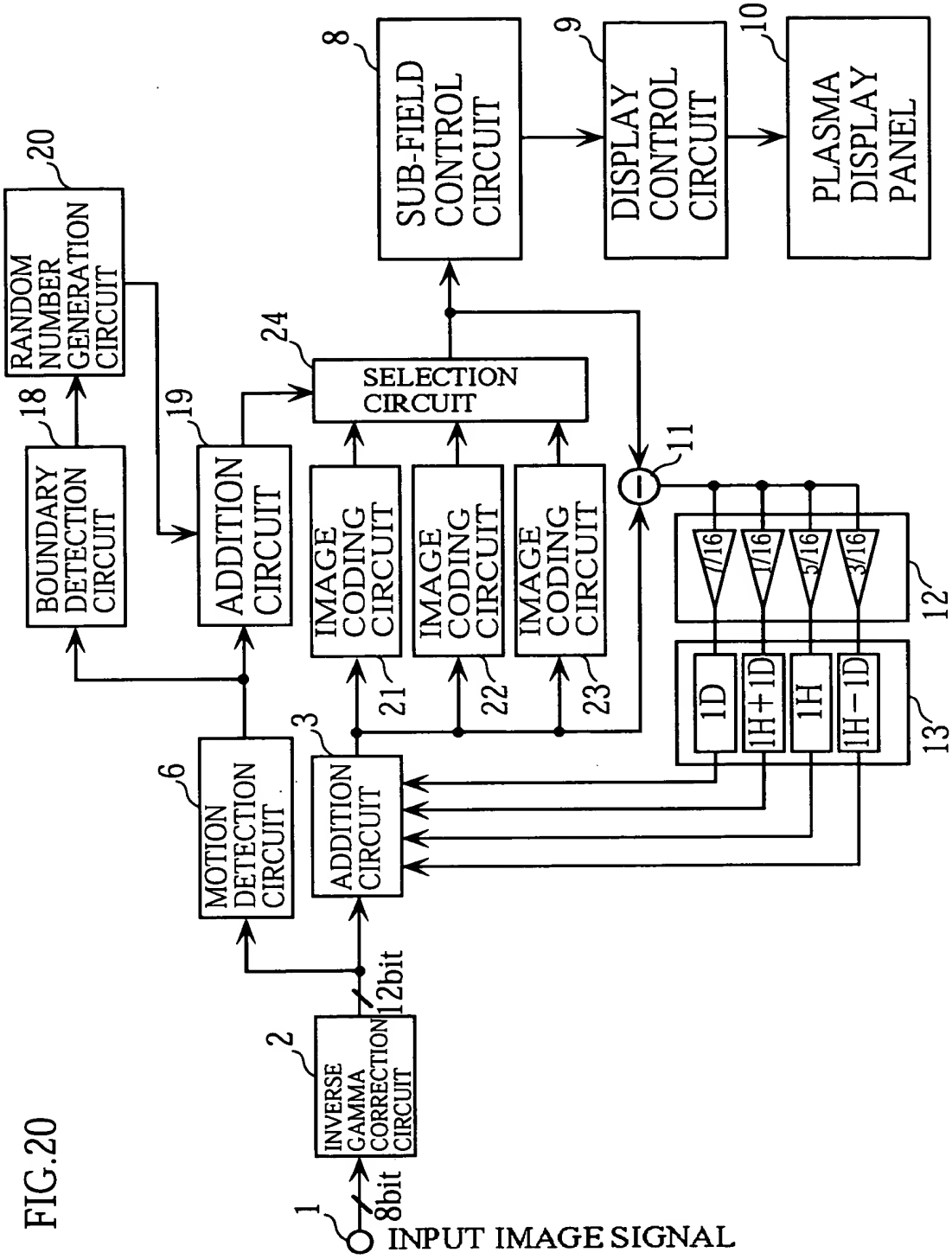

INPUT IMAGE SIGNAL
8bit
12bit
INVERSE GAMMA CORRECTION CIRCUIT
MOTION DETECTION CIRCUIT
ADDITION CIRCUIT
ADDITION CIRCUIT
BOUNDARY DETECTION CIRCUIT
RANDOM NUMBER GENERATION CIRCUIT
IMAGE CODING CIRCUIT
IMAGE CODING CIRCUIT
IMAGE CODING CIRCUIT
SELECTION CIRCUIT
SUB-FIELD CONTROL CIRCUIT
DISPLAY CONTROL CIRCUIT
PLASMA DISPLAY PANEL
7/16
7/16
5/16
3/16
1D
1H+1D
1H
1H−1D
1
2
3
6
8
9
10
11
12
13
18
19
20
21
22
23
24

FIG.20

FIG.21

(a)

INPUT LEVEL	SUB-FIELD LUMINANCE WEIGHTING							
	1	2	4	8	16	32	64	128
0								
1	1							
2		1						
3	1	1						
4			1					
5	1		1					
…								
31	1	1	1	1	1			
32						1		
…								
63	1	1	1	1	1	1		
64							1	
65	1						1	
…								
127	1	1	1	1	1	1	1	
128								1
129	1							1
…								
254		1	1	1	1	1	1	1
255	1	1	1	1	1	1	1	1

(b)

INPUT LEVEL	SUB-FIELD LUMINANCE WEIGHTING							
	1	2	4	8	16	32	64	128
0								
1	1							
2		1						
3	1	1						
4			1					
5−6	1		1					
7−8	1	1	1					
9−12	1	1		1				
13−18	1	1	1	1				
19−26	1	1	1		1			
27−38	1	1	1	1	1			
39−54	1	1	1	1		1		
55−78	1	1	1	1	1	1		
79−110	1	1	1	1	1		1	
111−158	1	1	1	1	1	1	1	
159−222	1	1	1	1	1	1		1
223−255	1	1	1	1	1	1	1	1

(c)

INPUT LEVEL	SUB-FIELD LUMINANCE WEIGHTING							
	1	2	4	8	16	32	64	128
0								
1−2	1							
3−5	1	1						
6−11	1	1	1					
12−23	1	1	1	1				
24−47	1	1	1	1	1			
48−95	1	1	1	1	1	1		
96−191	1	1	1	1	1	1	1	
192−255	1	1	1	1	1	1	1	1

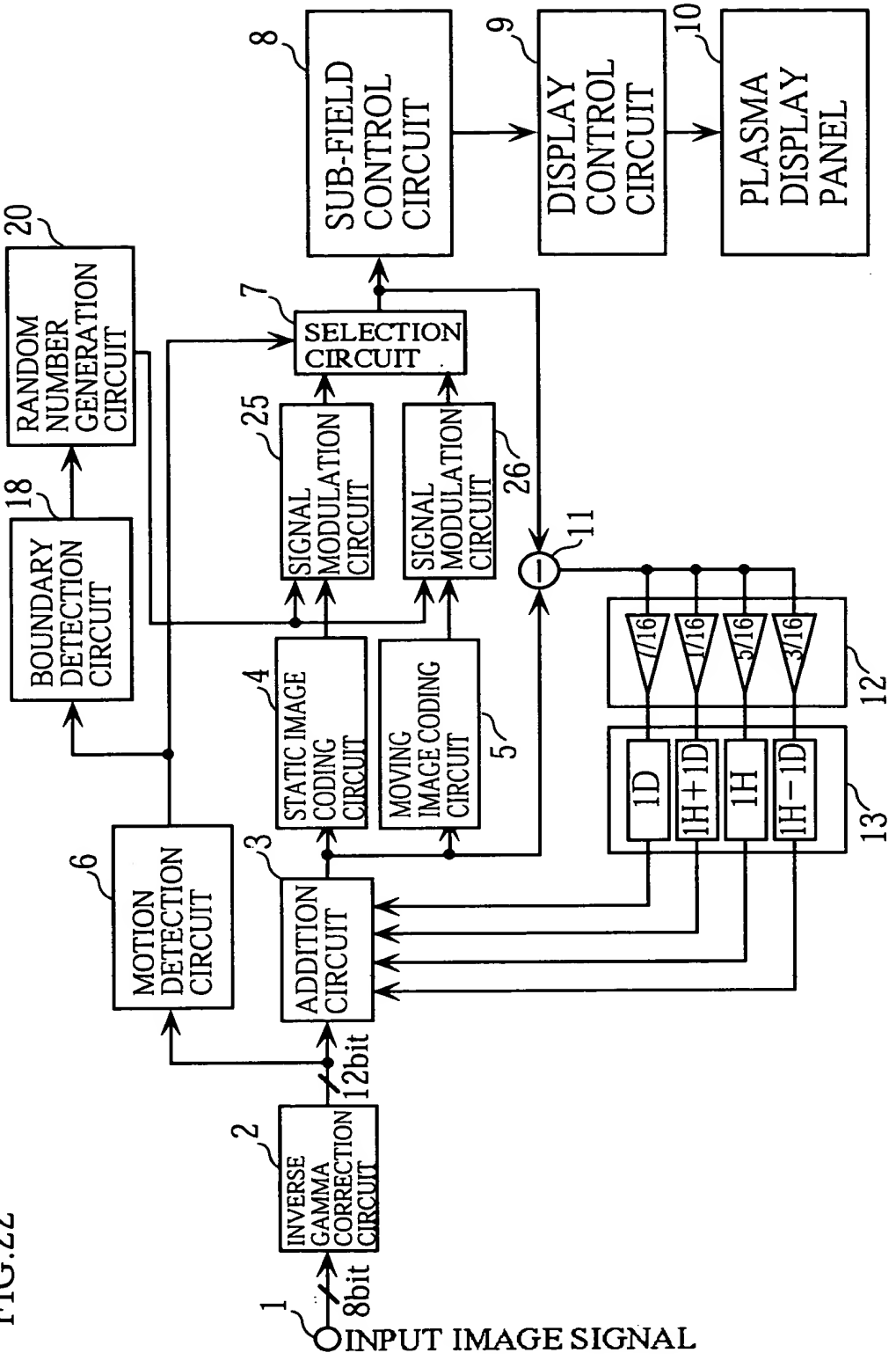

1
8bit
INPUT IMAGE SIGNAL
2
INVERSE GAMMA CORRECTION CIRCUIT
12bit
3
ADDITION CIRCUIT
6
MOTION DETECTION CIRCUIT
4
STATIC IMAGE CODING CIRCUIT
5
MOVING IMAGE CODING CIRCUIT
18
BOUNDARY DETECTION CIRCUIT
20
RANDOM NUMBER GENERATION CIRCUIT
25
SIGNAL MODULATION CIRCUIT
26
SIGNAL MODULATION CIRCUIT
7
SELECTION CIRCUIT
11
12
7/16
7/16
5/16
3/16
13
1D
1H+1D
1H
1H−1D
8
SUB-FIELD CONTROL CIRCUIT
9
DISPLAY CONTROL CIRCUIT
10
PLASMA DISPLAY PANEL

FIG.22

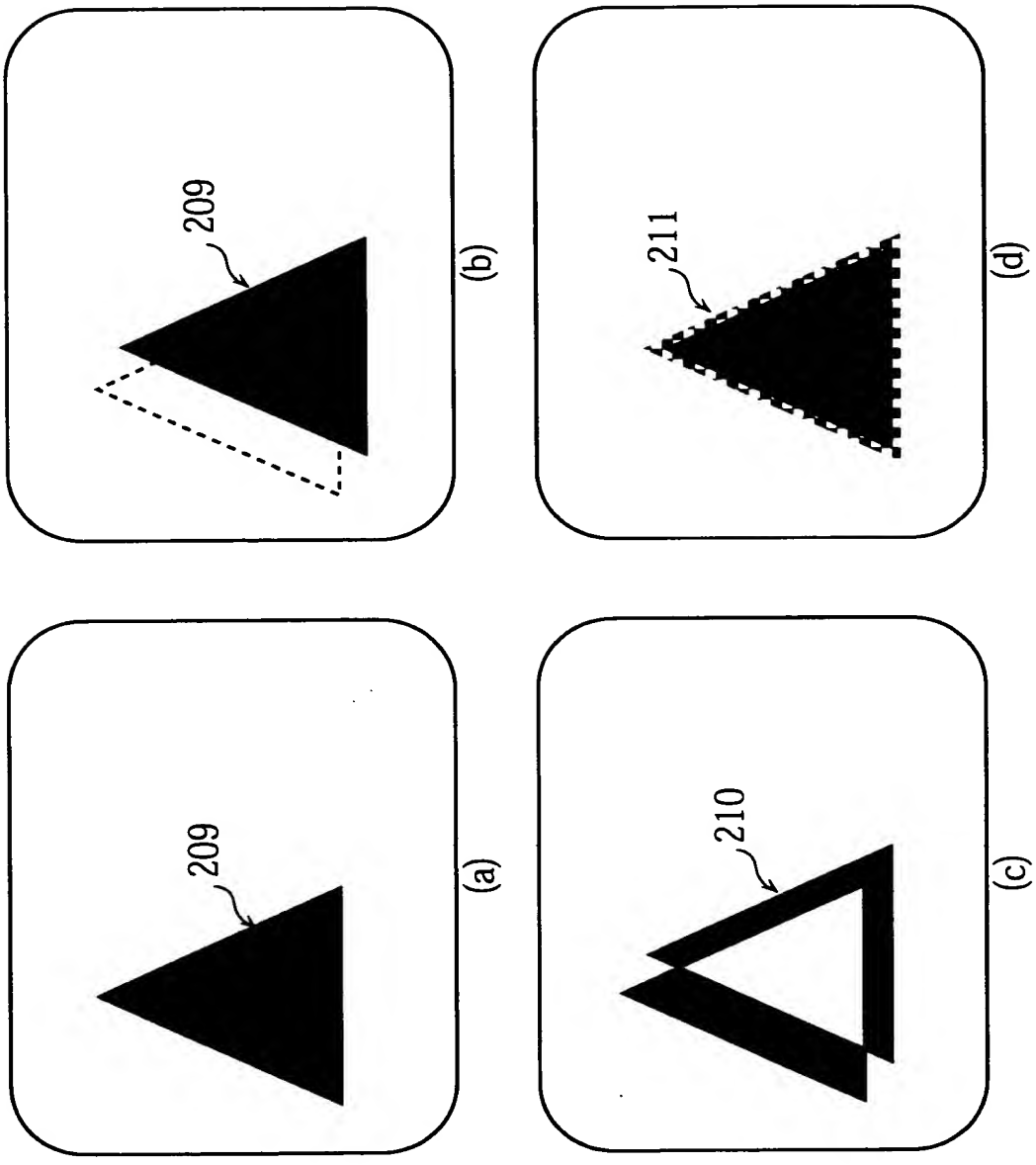


FIG.23

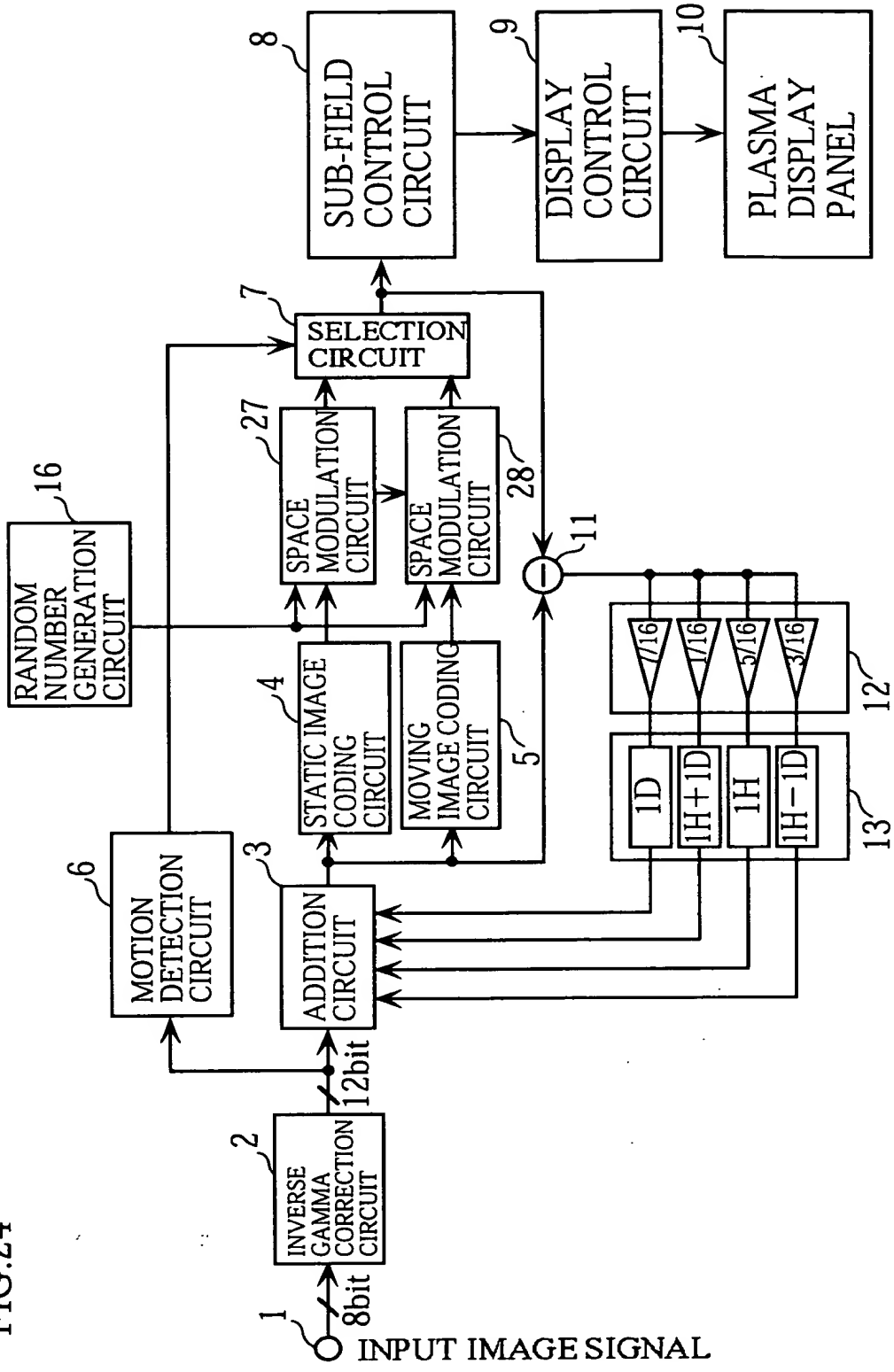

INPUT IMAGE SIGNAL
8bit
12bit
INVERSE GAMMA CORRECTION CIRCUIT
MOTION DETECTION CIRCUIT
ADDITION CIRCUIT
STATIC IMAGE CODING CIRCUIT
MOVING IMAGE CODING CIRCUIT
RANDOM NUMBER GENERATION CIRCUIT
SPACE MODULATION CIRCUIT
SPACE MODULATION CIRCUIT
SELECTION CIRCUIT
SUB-FIELD CONTROL CIRCUIT
DISPLAY CONTROL CIRCUIT
PLASMA DISPLAY PANEL
7/16
1/16
5/16
3/16
1D
1H+1D
1H
1H−1D
1
2
3
4
5
6
7
8
9
10
11
12
13
16
27
28

FIG.24

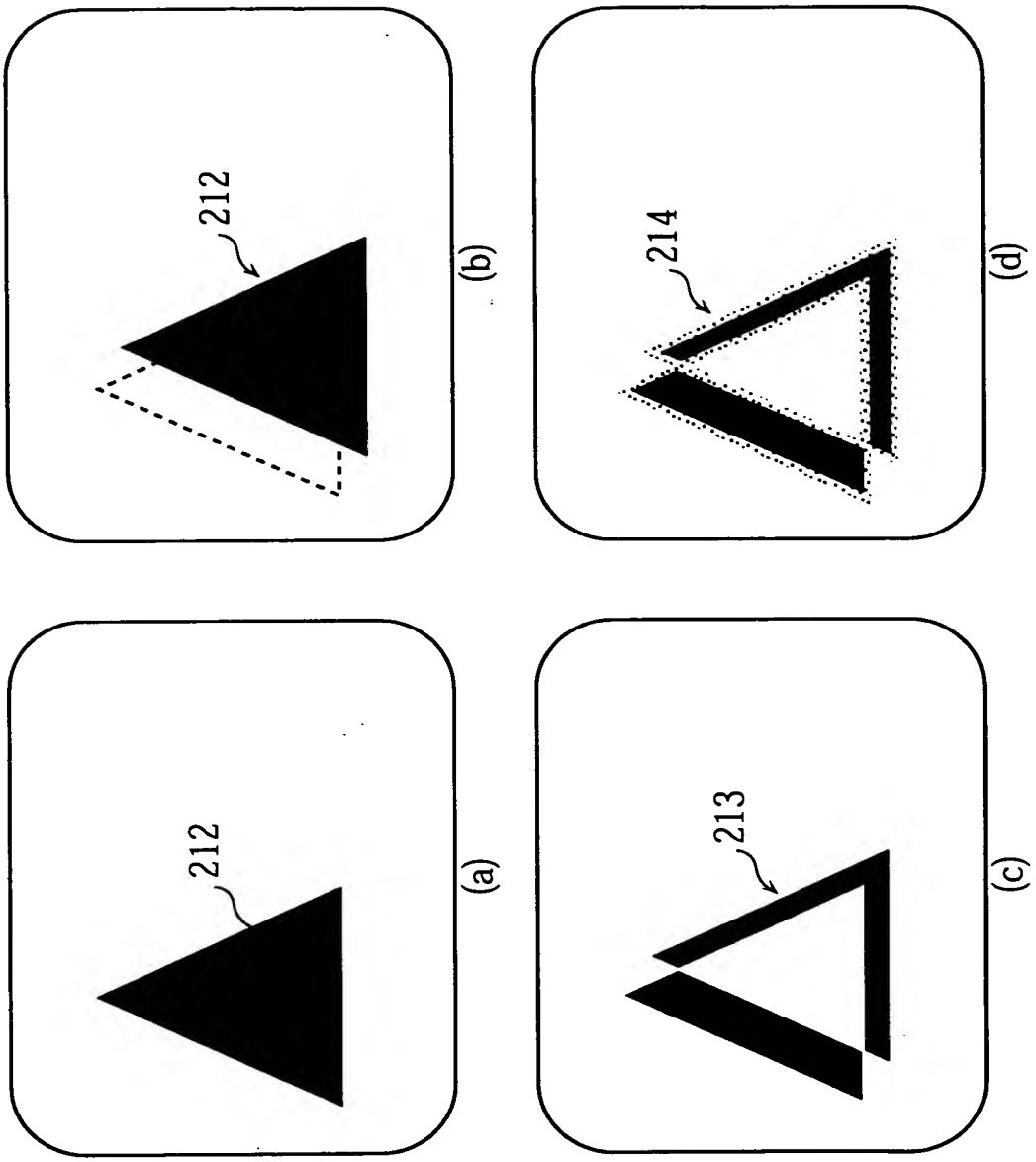


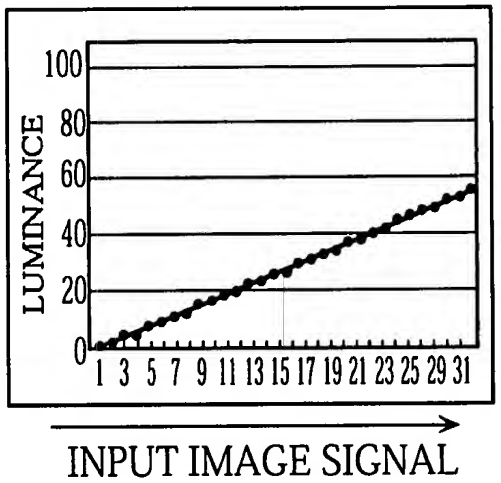
FIG.25

FIG.26

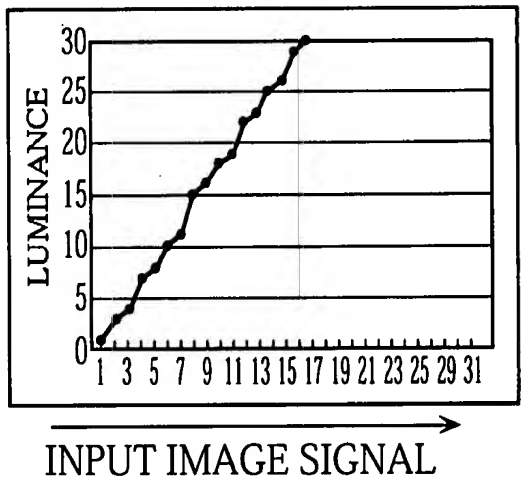
(a)

	INPUT IMAGE SIGNAL	SF1 1	SF2 3	SF3 7	SF4 15	SF5 29
	0					
	1	1				
	3		1			
	4	1	1			
	7			1		
	8	1		1		
	10		1	1		
	11	1	1	1		
★	15				1	
★	16	1			1	
	18		1		1	
	19	1	1		1	
	22			1	1	
	23	1		1	1	
	25		1	1	1	
	26	1	1	1	1	
★	29					1
★	30	1				1
★	32		1			1
★	33	1	1			1
	36			1		1
	37	1		1		1
	39		1	1		1
	40	1	1	1		1
★	44				1	1
	45	1			1	1
	47		1		1	1
	48	1	1		1	1
	51			1	1	1
	52	1		1	1	1
	54		1	1	1	1
	55	1	1	1	1	1

(b)



(c)



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